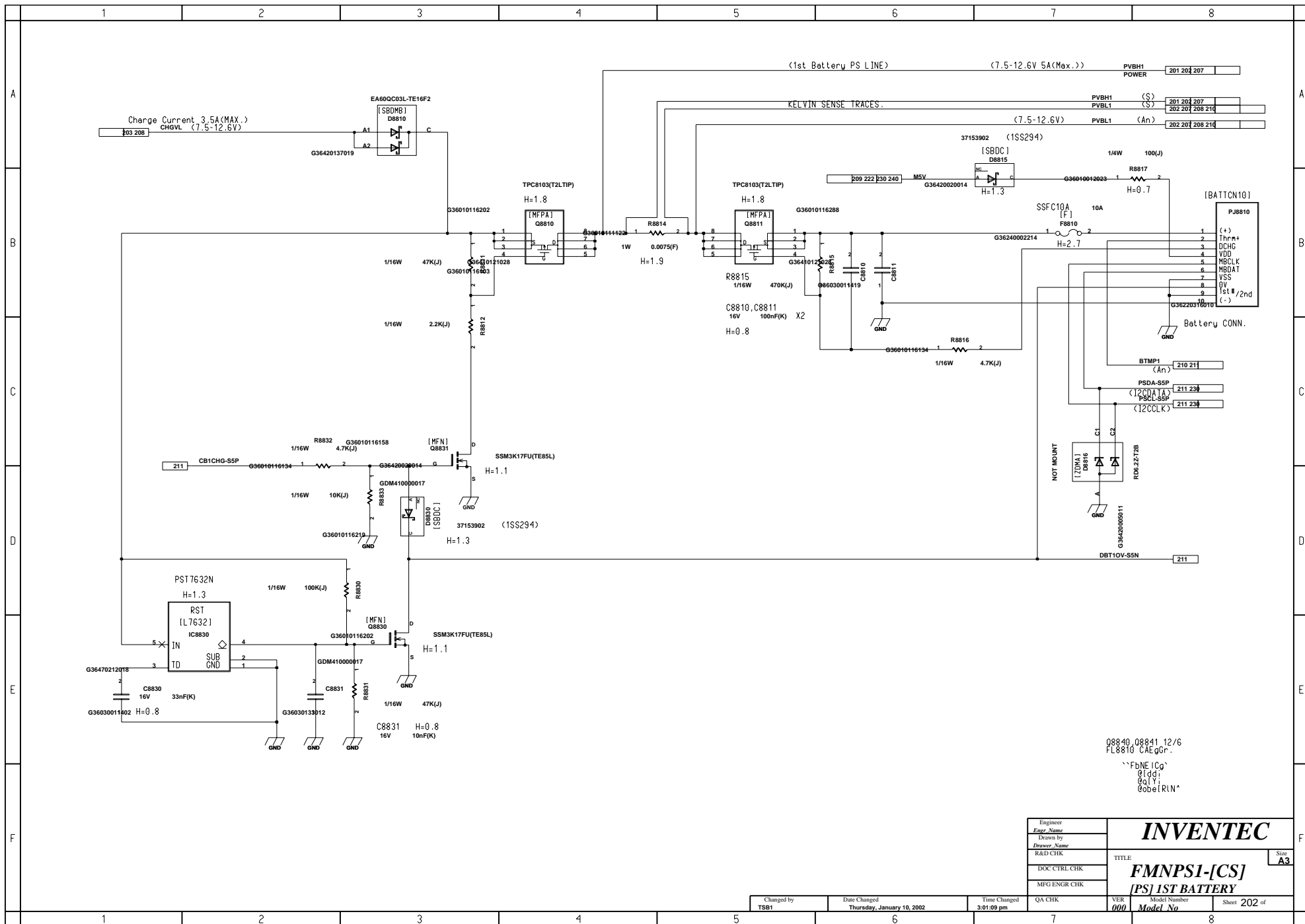


	1	2	3	4	5	6	7	8	
A									A
B									B
C									C
D									D
E									E
F									F

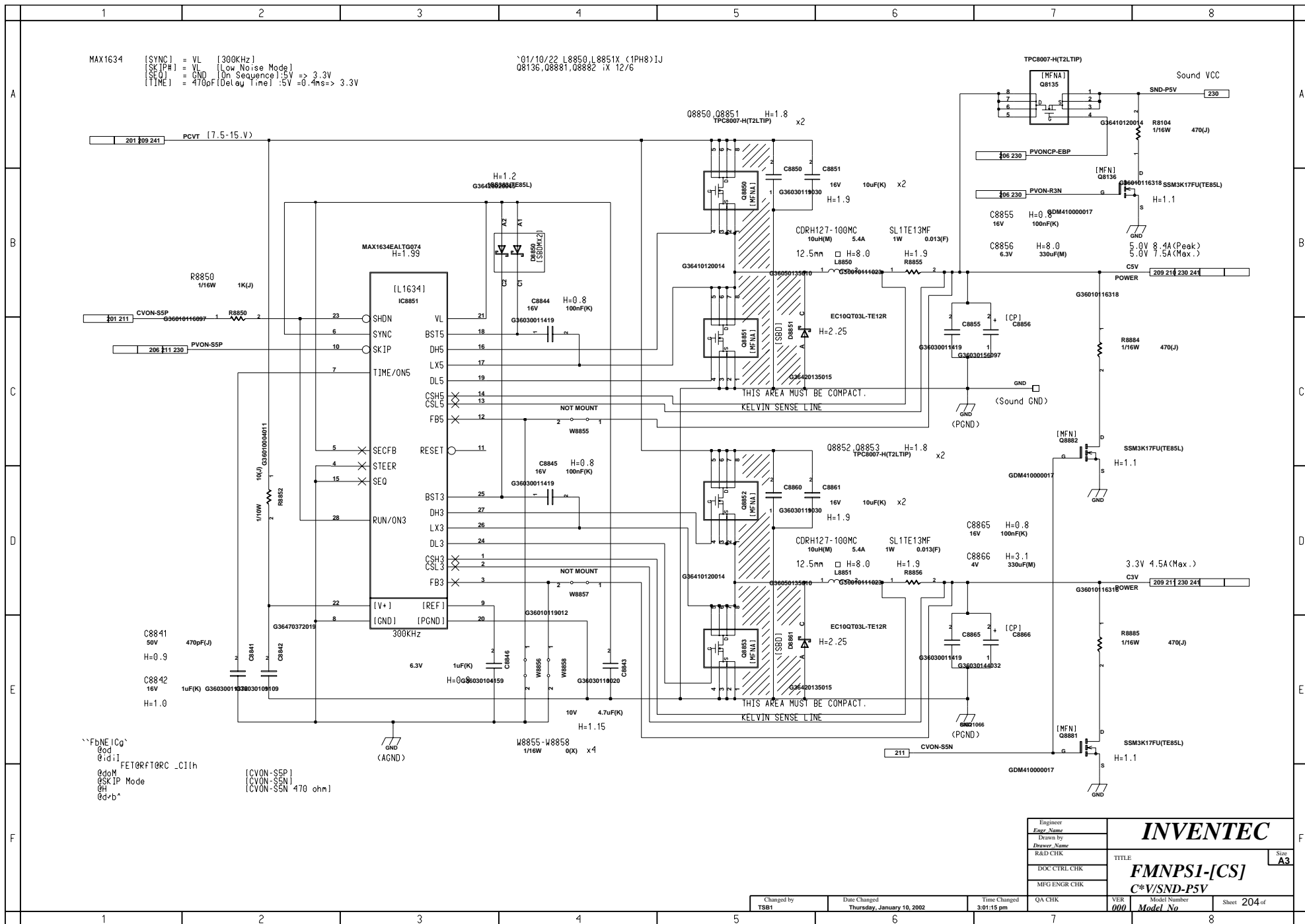
SHT.	Power Signal	Voltage	I Static	I Limit	Power on	SKIP Mode	Other
204	C3V	3.3V	4.5A		CV0N-S5N	PV0N-S5P	
205	E3V				EV0N-S5N		
	B3V				B15NCHBV		
	P3V				B15NCHPV		
204	C5V	5.0V	7.5A	8.4A	CV0N-S5N	PV0N-S5P	
205	E5V				EV0N-S5N		
	B5V				B15NCHBV		
	P5V				B15NCHPV		
	SND-P5V				PV0N-S5P		
206	15-EBV	11.5V	1mA		E5V		
209	S1V	1.8V	100mA		SV0N-S5N		
209	S3V	3.3V	100mA		SV0N-S5N		
209	S5V	5.0V	50mA		SV0N-S5N		
209	M5V	5.0V	100mA		PVD/PBV		
209	MCV	5.0V	25mA		PVD/PBV		
213	PPV	1.0	30.0A	40.0A	ONCPU-E3P	Disable	IMVP3
214		1.3V					
215	1R2-P1V	1.20V	300mA		ONVID-E5P		
216	2R5-E2V	2.51V	4.0A	4.0A	EV0N-S5P	Enable	
218	2R5-B2V				B15NCHBV		
217	1R25-E1V	2R5V/2	3.0A	3.0A	EV0N-S5P	PV0N-S5P	
218	1R25-B1V				B15NCHBV		
217	1R25VR-E1V	2R5V/2			EV0N-S5P		DDR t0Xpd
218	1R25VR-B1V				B15NCHBV		
219	1R5-E1V				EV0N-S5P		
218	1R5-P1V	1.51V	2.0A	3.0A	B15NCHPV	Enable	
220	1R8-E1V	1.81V	2.0A	3.0A	EV0N-S5P	Enable	
205	1R8-P1V				B15NCHPV		
221	FAN VCC	3.3V	400mA				
222	R3V	2.0`3.5V	0.1mA				
	VGA VCC(1)						VGA Core
	VGA VCC(2)						VGA VRAM

Engineer				INVENTEC	Size A3
Engr Name					
Drawn by					
Drawer Name					
R&D CHK					
DOC CTRL CHK				TITLE: FMNPS1-[CS]	Model Number
MFG ENGR CHK					
Changed by TSB1	Date Changed Thursday, January 10, 2002	Time Changed 3:00:37 pm	QA CHK	VER 000	Sheet 200 of





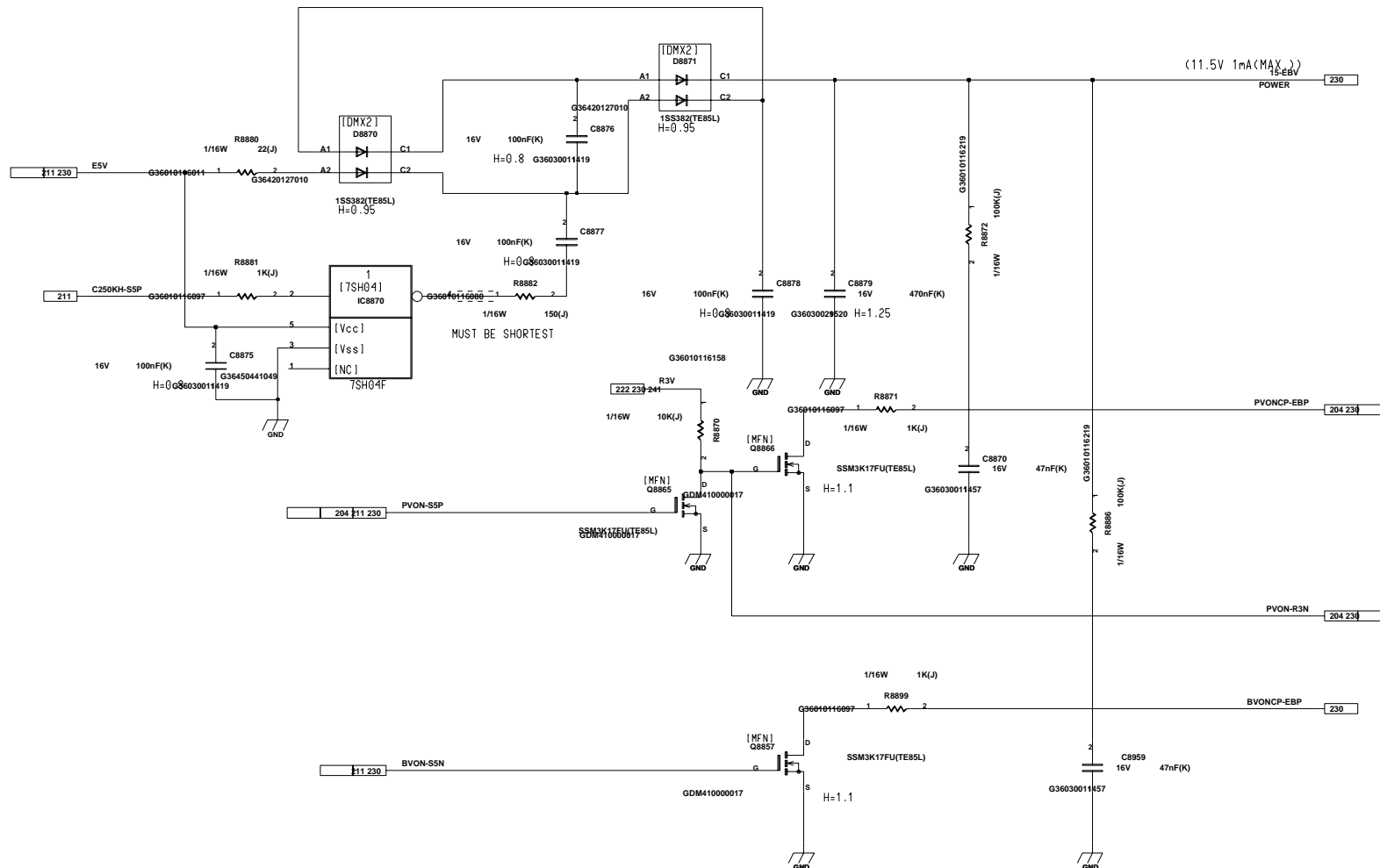
Engineer <i>Engnr Name</i>	<div style="text-align: center;"> <h1>INVENTEC</h1> </div>			<div style="text-align: right;"> State A3 </div>	
Drawn by <i>Drawer Name</i>					
R&D CHK					
DOC CTRL CHK					
MFG ENGR CHK	TITLE	<div style="text-align: center;"> <h2>FMNPS1-[CS] [PS] 2ND BATTERY</h2> </div>			
QA CHK	VER 000	Model Number Model_No	Sheet 203 of		



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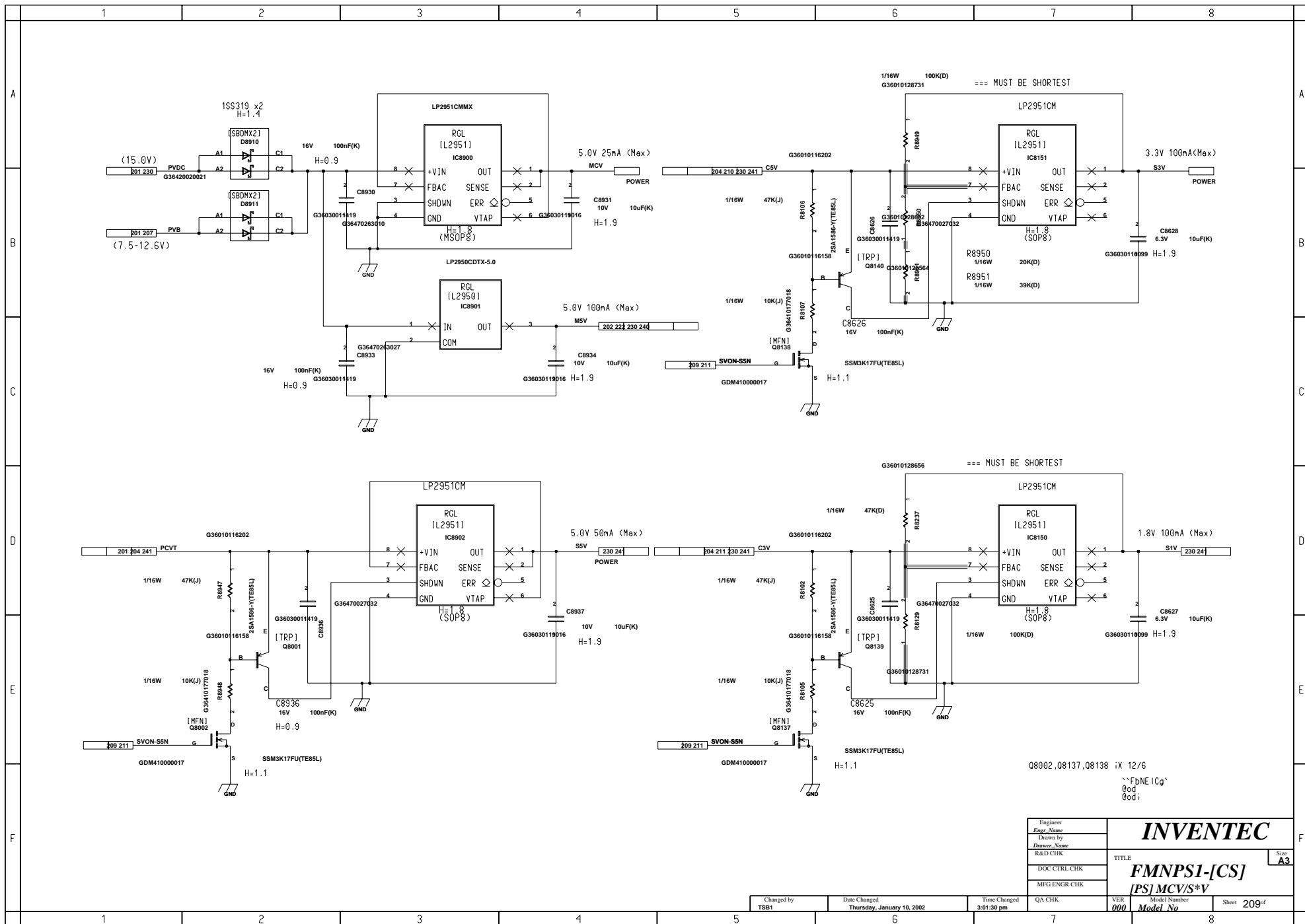
`FbNE ICg`
@od
@odiv(1.0mA)
@rl (PULL UP)
@qGSL(FETQ1g)
@o(100k + 47nF)

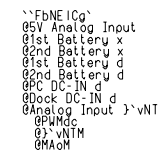
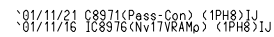
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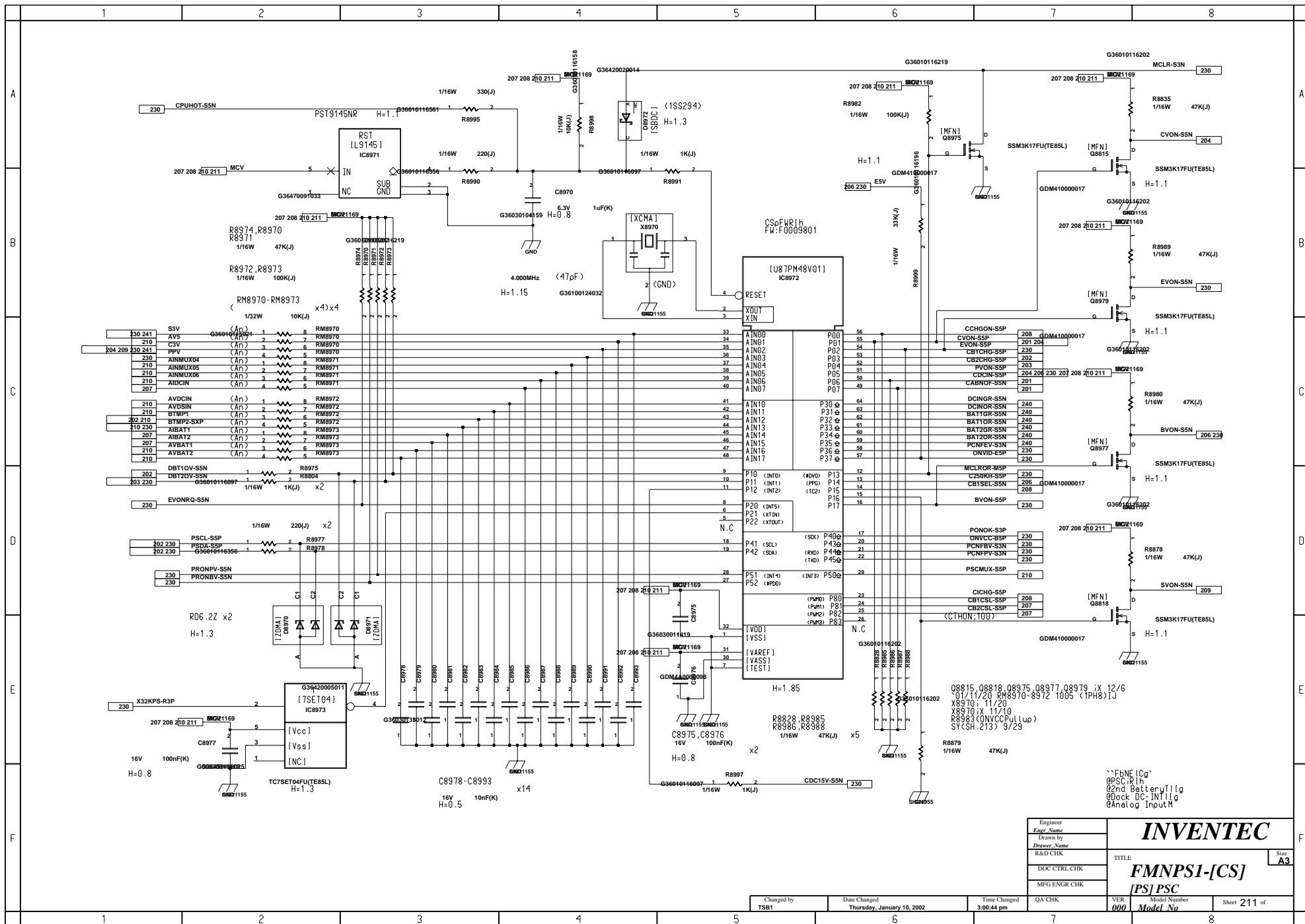
Q8857, Q8865, Q8866 : X 12/6

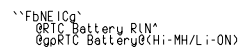
Engineer <i>Engr. Name</i>	<div>INVENTEC</div> <div>TITLE: <i>FMNPS1-[CS]</i> <i>[PS] E15V</i></div>			Size A3
Drawn by <i>Drawer Name</i>				
R&D CHK				
DOC CTRL CHK				
MFG ENGR CHK				
QA CHK	VER 000	Model Number <i>Model No</i>	Sheet	206 of





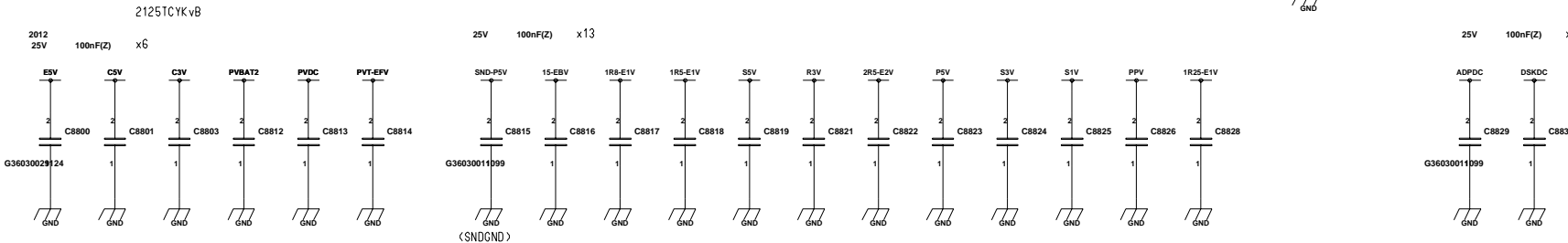
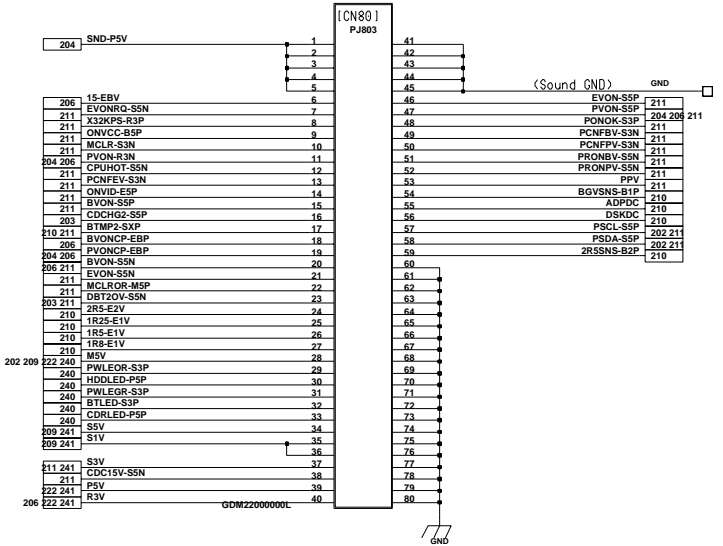
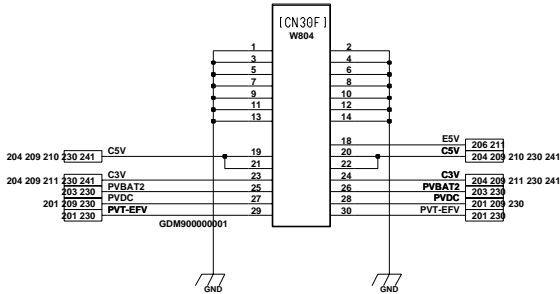
Changed by TSB1	Date Changed Thursday, January 10, 2002	Time Changed 3:00:40 pm	QA CHK	VER 000	Model Number Model No	Sheet 210 of
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Changed by TSB1	Date Changed Thursday, January 10, 2002	Time Changed 3:00:47 pm	QA CHK	VER 000	Model Number Model No	Sheet 222 of
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01/12/05 1PH8-CR-01B020 (38PinCDC15V-S5N) (1PH8)IJ

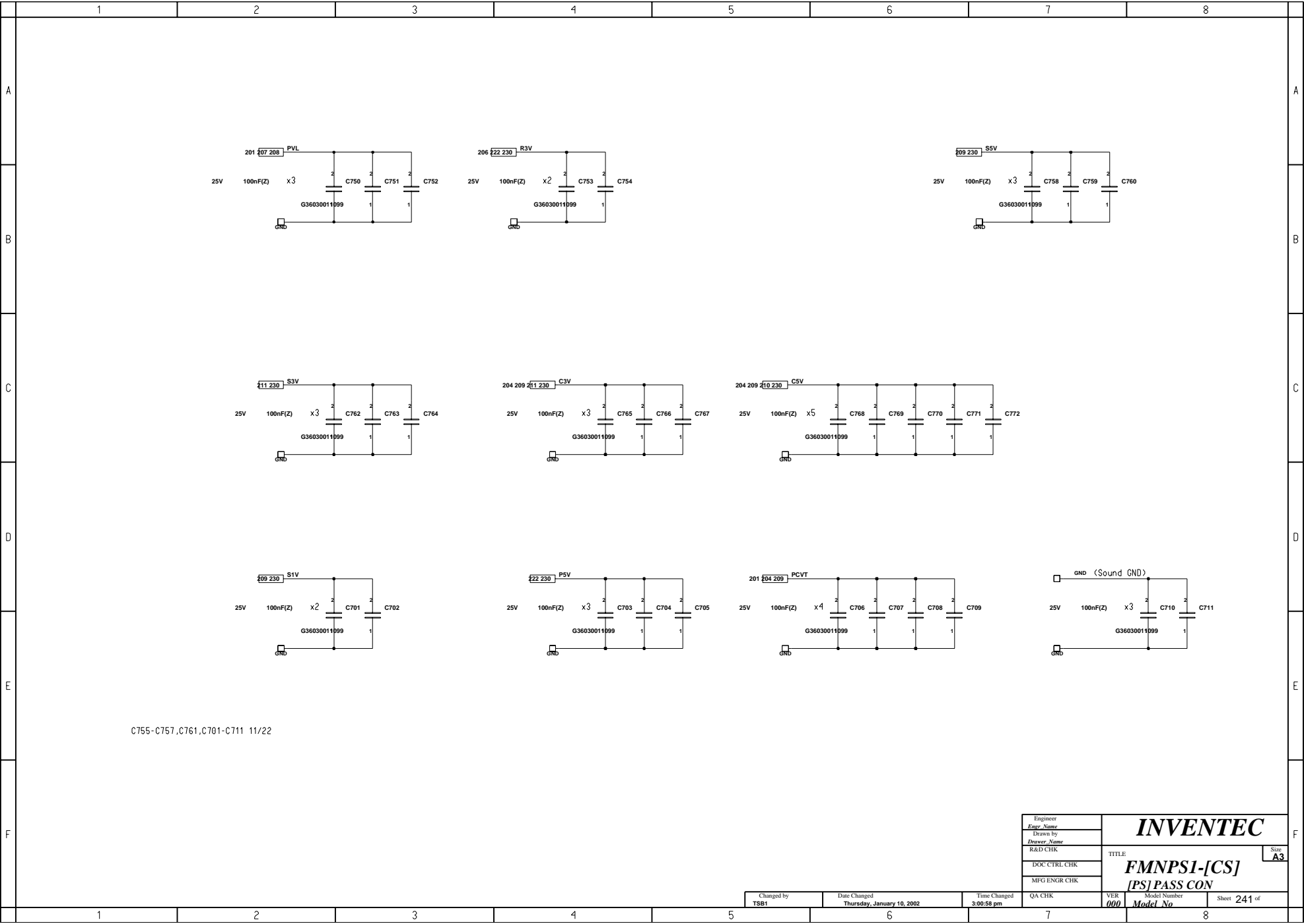


C88151P1NGDX 11/22
BGVGVSN5-B1PXAC8827A
PJ803 S3P IN2R5-B20 11/16
REF:Montreal10(frops2 rev.00)

FbNICg KyMATICFbN
0h'eFbN

Engineer Engr Name	INVENTEC
Drawn by Drawer Name	
R&D CHK	
DOC CTRL CHK	
MFG ENGR CHK	
TITLE: FMNPS1-[CS]	
[PS] SYS(FMNSY*) I/F	
Model Number Model No	Sheet 230 of

Changed by TSB1	Date Changed Thursday, January 10, 2002	Time Changed 3:00:50 pm
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Engineer <i>Engr Name</i>	<div>INVENTEC</div> <div>TITLE: FMNPS1-[CS]</div> <div>[PS] PASS CON</div>			Size A3		
Drawn by <i>Drawer Name</i>						
R&D CHK						
DOC CTRL CHK						
MFG ENGR CHK						
Changed by TSB1	Date Changed Thursday, January 10, 2002	Time Changed 3:00:58 pm	QA CHK	VER 000	Model Number Model No	Sheet 241 of